#13 Appeal Brief
M. Brunsen
9/25/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Shuichi Kikuchi et al.
Serial No. : 09/444,819
Filed : November 22, 1999
Title : SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

Art Unit : 2814
Examiner : Shrinivas H. Rao

BOX AF
Commissioner for Patents
Washington, D.C. 20231

BRIEF ON APPEAL

A Notice of Appeal was filed June 13, 2002. A petition and a fee for a one-month extension is attached.

(1) Real Party in Interest

The real party of interest is Sanyo Electric Co. Ltd., the assignee of the pending application.

(2) Related Appeals and Interferences

None

(3) Status of Claims

Claims 1-4, 8-10, 17, and 19 are pending. Claims 1 and 2 were finally rejected under 35 USC §102(e) as being anticipated by US Patent No. 6,127,700 (Bulucea). Claims 3, 4, 8-10, 17, and 19 as being unpatentable under 35 USC §103(a) over Bulucea as applied to claims 1 and 2 , and further in view of US Patent No. 5,869,371 (Blanchard).

The Applicants appeals the rejection of claims 1-4, 8-10, 17, and 19.

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I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

September 13, 2002
Date of Deposit

Kathryn Lugo
Signature

KATHRYN LUGO
Typed or Printed Name of Person Signing Certificate

(4) Status of Amendments

No amendments were made in the response to the Final Office Action.

(5) Summary of Invention

The subject matter of the pending claims relates to a semiconductor device that includes a source region, a channel region, a drain region, a gate electrode disposed above the channel region, and a drift region disposed adjacent to the channel region and extending to and below the drain region. The drift region is formed shallowly at least below the gate electrode but formed deeply in a neighborhood of the drain region.

The drift region 22, illustrated in an embodiment (A) of Fig. 1 (A), includes the shallow portion 22A below the gate electrode 7 and the deep portion 22B around and below the drain region 5.

(6) Issues

Whether claims 1 and 2 were properly rejected under 35 USC §102(e) as being anticipated by US Patent No. 6,127,700 (Bulucea), and whether claims 3, 4, 8-10, 17, and 19 were properly rejected as being unpatentable over Bulucea as applied to claims 1 and 2 , and further in view of US Patent No. 5,869,371 (Blanchard).

(7) Grouping of Claims

Claims 1, 2, 8, and 9 are independent from each other. Claims 1 and 17 stand or fall together. Claims 2, 3, 4, and 19 stand or fall together. Claim 8 stands or falls by itself. Claims 9 and 10 stand or fall together.

(8) Argument

Response to the Final Office Action

Claims 1 and 2 have been rejected under 35 USC 102(e) as being anticipated by Bulucea.

On page 3 of the Final Office Action dated December 14, 2001, it is alleged that Bulucea discloses "a drain region (Fig. 13, #135, col. 20, line 5), ... a drift region (Fig. 13, #136; col. 20, line 7) adjacent to the channel region and extending to and below the drain region, wherein the drift region (136) is formed shallowly at least below the gate electrode but formed deeply in a neighborhood of the drain region (Fig. 13)."

However, Bulucea does not teach this as alleged in the Final Office Action. First, the lightly doped extension 136, which the Examiner equates with the present invention's drift region, is not a drift region but a drain region. In column 20, lines 4 to 6, Bulucea states referring to Fig. 13 that "the FET 130 has (a) a source zone formed with... and (b) a drain zone formed with n++ main portion 135 and more lightly doped n+ extension 136." It is clear from this statement that both portion 135 and extension 136 make up the drain zone (region). Clearly, the extension 136 is not a drift region as asserted in the Final Office Action.

Second, claim 1 states "a drift region ... **extending to and below the drain region,** wherein the **drift region is** formed shallowly at least below the gate electrode but **formed deeply in a neighborhood of the drain region**." Bulucea's Fig. 13 (or any other figures) does not disclose any drift region extending to and below the drain region and formed deeply in a neighborhood of the drain region. In fact, Bulucea is completely silent as to where the drift region is. Even assuming *arguendo* that the extension 136 is a drift region as alleged in the Final Office Action, Fig. 13 shows this extension to be adjacent to the main portion 135 but not extending to and below the main portion 135 or being deeply in a neighborhood of the main portion 135.

For each of the two above reasons, claim 1 is not anticipated by Bulucea. Substantially the same distinction can be made with other independent claims 2, 8, and 9.

Independent claim 2 also is not anticipated by Bulucea. The drift region of claim 2 is formed shallowly from the channel region to the drain region, at least below the gate electrode, and formed deeply in the neighborhood of the drain region. That is, the drift region of claim 2 exists in two different and distinct depth levels in the substrate (as is the case for claim 1). None

of Bulucea's cited figures, including Figs. 12 to 14, show a drift region that is formed shallowly next to a channel region and formed deeply in the neighborhood of a drain region. For example, Fig. 12 shows a p-type drain region consisting of a main portion 85 and an extension 86, which is adjacent to the main portion. No drift region is shown. Even assuming *arguendo* that the extension 86 is a drift region, it does not exist in two different depth levels -- shallowly from the channel region to the drain region and deeply in the neighborhood in the drain region -- as claimed in claim 2. Other Bulucea figures similarly do not show the features of claim 2 as described above.

For completeness, it should be mentioned that the threshold body region 67 in Bulucea's Fig. 12k is p-type and is next to and partly under the source zone 63/64, which is n-type. The region 67 thus does not correspond to the drift region of claim 1 or 2. Even assuming *arguendo* that the bias is reversed such that source zone 63/64 is made into a drain zone and the threshold body region 67 is assumed to be a "drift" region, the region 67 still does not correspond to the present invention's drift region because (1) the body region 67 does not have a two-level depth structure of claim 1 or 2, and (2) the drain and the drift regions of claim 2 are made of the same conduction type, whereas the threshold body region 67 and the zone 63/64 are made of the opposite types (p-type and n-type). Other figures including Figs. 13 and 14 similarly do not show the drift region of the present invention for the reason stated above.

Claims 3-4, 8-10, 17 and 19 have been rejected as being unpatentable over Bulucea as applied to claims 1 and 2, and further in view of Blanchard. In response, the Applicants point out that Bulucea does not disclose, teach, or suggest a drift region formed by three different kinds of implants.

In rejecting claim 3, it is alleged in the Final Office Action that Bulucea teaches arsenic implantation in column 17, line 26; phosphorous implantation in column 18, line 34; and boron implantation in column 19, line 34. In particular, Bulucea and Blanchard alone or in combination does not teach the claimed second conductivity type **drift region** "formed by implanting at least two kinds of second conductivity type impurities which have different

diffusion coefficients and at least one kind of first conductivity type impurity which has a diffusion coefficient substantially equal to or larger than the diffusion coefficient of at least one kind of second conductivity type impurity..." (claim 3). The effect of this is to create (1) a deep drift region where one, second conductivity type impurity with a greater diffusion coefficient is made to penetrate deeper into the substrate and (2) a shallow drift region where the second conductivity type impurity in the deeper region is canceled by the first conductivity type impurity. That is, the claimed second conductivity type drift region is made of at least three kinds of implantations. Bulucea's implantation passages cited by the Examiner refer to the formation of the source and the drain regions (see Figs. 12 a to 12n; and column15, line 23 to column 19, line 40). Bulucea does not mention anything about forming a drift region.

Furthermore, Blanchard also does not teach or suggest the above cited feature of claim 3. Blanchard in column 4, lines 2 to 7, gives the dose and the energy needed to form the boron implanted p+ diffusions 106. There is also a mention of a shallow n- arsenic implant or replacing this arsenic with other antimony implants (column 10, lines 1 to 5). In Blanchard, arsenic is used to create a source region 126 (column 4, line 66 to column 5, line 3) and boron is used to create a body region 124 (column 4, lines 61 to 65). In column 10, lines 1 to 5, Blanchard merely suggests that arsenic may be replaced with other antimony implants or other dopants may be changed to other species. There is no teaching or suggestion in Blanchard of making the drift region with three kinds of implants. Bulucea in view of Blanchard does not teach or suggest the compositions of claim 3. Thus, a person of ordinary skill in the art would not have found obvious the invention as claimed in claim 3.

Bulucea and Blanchard also do not teach or suggest a feature of claim 4 for much of the same reason as above. Claim 4 recites that "the second conductivity type drift region is formed by implanting an arsenic ion and a phosphorous ion as the second conductivity type impurities into an overall surface of a region serving as a drift region and selectively implanting a boron ion as the first conductivity type impurity only into a region in a neighborhood of the source region." Both Bulucea and Blanchard do not teach or suggest the drift region of claim 4 formed of

arsenic, phosphorous and boron. Thus, at least for the foregoing reason, claim 4 is not made obvious by Bulucea in view of Blanchard.

It is submitted that claims 8 and 9 that have the same drift region feature of claim 1 are not obvious at least for the same reasons as claim 1. Additionally, dependent claims 3, 4, 10, 17 and 19 are not obvious at least for the same reasons as independent claims 1, 2, 8, or 9 from which they depend.

Furthermore, with respect to claims 8 and 9, the Final Office Action merely states without any reason or recitation that Bulucea teaches a second MOS transistor with a low concentration source-drain region formed adjacent to the second gate electrode, a high concentration source-drain region, and a middle concentration source/drain region. The Applicants do not find that teaching in Bulucea and the Examiner did not point to such a teaching. Thus, a person of ordinary skill in the art would not have the invention as claimed in claims 8 and 9 obvious.

Thus, all pending claims 1 to 4, 8 to 10, 17 and 19 are novel and patentable for the foregoing reasons.

Further Response to the Advisory Action

In the Advisory Action dated April 30, 2002, the Examiner further elaborated and presented new arguments to our response to the Final Office Action. The Applicants disagree with the arguments in the Advisory Action on all counts as we submit below.

In the Advisory, it is stated that "Applicants' arguments that Bulucea's element 136 is not a drift region is not persuasive because drift region is defined as a region wherein the electrons/holes move in random motion due to the applied electric field and applying the broadest reasonable interpretation, element 136 in Fig. 13 of Bulucea which illustrates a FET, is a drift region."

First, the Applicants point out that it is the claims that are given the broadest possible interpretation, not the prior art. *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969) (During patent examination, the pending claims must be given the broadest reasonable interpretation consistent with the specification).

Second, the interpretation in the Advisory is not consistent with the description of the region 136 as part of the "drain zone" in Bulucea. As stated before, in column 20, lines 4 to 6, Bulucea states referring to Fig. 13 that "the FET 130 has ... a drain zone formed with n++ main portion 135 and more lightly doped n+ extension 136." It is clear from this statement that the both the portion 135 and the extension 136 make up the drain zone (region). It is technically erroneous to equate the drain region with the drift region. The drift region does not necessarily overlap with the drain region, as it is clear from the description and in the figures in the present application (see, for example, page 4, lines 18 to 27 and Fig. 1). Bulucea lacks a description of where any drift region is in his figures or description.

Moreover, the drain and drift regions are not merely a matter of semantics or nomenclature. In his June 2002 article, "LDMOS Turns Up the Power," in *Compound Semiconductor*, Robert Metzger states:

> The high operating voltages required for power-amplifier applications are achieved through **optimized design of the drift region between the gate and the drain** of the LDMOS transistor. To achieve high breakdown characteristics, the typical LDMOS design relies on a drift region formed by an n-type diffusion well placed in a p-type substrate. (Emphasis added.) (*Compound Semiconductor*, Vol. 8, No 5, p. 33, June 2002.)

The structural design of a drift region apart from the drain region is important to the performance of the device. The drain and the drift regions are different and distinct regions configured to perform different functions. To paraphrase Metzger, the design of the drift region apart from the drain region is crucial in achieving a particular breakdown voltage characteristic in LDMOS. Bulucea's drain structure (not the drift region) was used to achieve his particular

voltage characteristics. In contrast, the two-tier structure of the drift region of the present invention was designed to achieve its own breakdown voltage characteristics. Arbitrarily stating that Bulucea's drain region 136 is a drift region, when Bulucea clearly states otherwise, is grounded on no other reason than to reject the present invention by impermissibly using flawed hindsight.

use limitation in device claims

It is further stated in the Advisory that "[e]ven the applicant's in their specification page 8, lines 5-7, etc. describes their region 22 as a drift region which is identical to Belucea's region 136."

The point of this argument is not understood. The description on page 8, lines 5 to 7 describes an embodiment of the present invention. The region 22 is a drift region as claimed in the present application and is consistent with the applicants' previous assertion that it is not identical or similar to Bulucea's region 136. This point is further clarified by the argument following the Examiner's quote below.

"Further Bulucea in Fig. 6 describes the drift region extending to and below the drain region and is formed shallowly below the gate electrode and deeply in the neighborhood of the drain region."

Bulucea's Fig. 6 or any other figures do not disclose a drift region extending to and below the drain region and is formed shallowly below the gate electrode and deeply in the neighborhood of the drain region, as presently claimed in claim 1 and similarly in claim 2 or 9. First of all, Fig. 6 does not describe a drift region; it only shows a drain region 52. Second, if we take the step suggested by the Examiner to assume that the drain 52 is a "drift" region, then an illogical result of not having any drain region is reached. If the extended part 53 of the drain region is assumed to be the drift region, then Fig. 6 does not show a drift region extending to and below a drain region and is formed shallowly below the gate electrode and deeply in the neighborhood of the drain region. That is, Fig. 6 does not show a drift region being formed below (i.e. deeply in a neighborhood of) the drain region and being formed shallowly below the electrode (a two-level drift region structure). Bulucea does not disclose, teach, or suggest the

drift region of the present invention of claim 1, 2 or 9. Similar arguments can be made against Bulucea's drain region 135, 136 in Fig. 13. The Examiner is impermissibly contorting the teaching of Bulucea inorder to conform to the claimed invention.

Thus, the anticipation rejection is founded upon improper hindsight and the improper use of the Applicants' own invention as a blueprint to contort the teaching of the prior art. Furthermore, for the foregoing reasons even assuming *arguendo* that Bulucea's drain region is a drift region, such a structure still does not anticipate the present claimed invention.

The Advisory continues on to state, "[s]ince region 136/64 are drift regions they both are the same conductivity as drain regions 135/63. With respect to claims 3-4, 10, 17 and 19 it is noted that applicants' are arguing a method step in a device claim and the method step cannot be given patentable weight."

The Applicants' assert that claims 3-4, 10, 17 and 19 are not method claims. Claims 3 and 4 claim a drift region that is formed by three different kinds of implants. Claims 10, 17, and 19 all claim structural elements.

Finally the Advisory states, "[f]urther these claims are rejected over Bulucea and Blanchard and Blanchard in col. 4 lines 61 –66 teaches global implants by arsenic and boron.' Bulucea in Figs. 10a etc. and col. 6 lines line 50 describes a BICMOS and it well know that BICMOS have two gate electrodes."

A rebuttal was fully made against this assertion on pages 4 and 5 herein.

Conclusion

The Applicants respectfully request that claims 1-4, 8-10, 17, and 19 be allowed.

The brief fee of $320 is enclosed. A petition and a fee of $110 for one-month extension are also enclosed. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 9/13/02

Chris T. Mizumoto
Reg. No. 42,899

Fish & Richardson P.C.
45 Rockefeller Plaza, Suite 2800
New York, New York 10111
Telephone: (212) 765-5070
Facsimile: (212) 258-2291

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Appendix of Claims

1. A semiconductor device comprising a source region, a channel region, a drain region, a gate electrode disposed above the channel region, and a drift region disposed adjacent to the channel region and extending to and below the drain region,

wherein the drift region is formed shallowly at least below the gate electrode but formed deeply in a neighborhood of the drain region.

2. A semiconductor device comprising:

a first conductivity type well region formed in a first conductivity type semiconductor substrate;

a gate electrode formed on the substrate via a gate insulating film;

a first conductivity type body region formed to be adjacent to the gate electrode;

a second conductivity type source region and a channel region formed in the first conductivity type body region;

a second conductivity type drain region formed at a position remote from the first conductivity type body region; and

a second conductivity type drift region formed shallowly from the channel region to the drain region, at least below the gate electrode, and formed deeply in a neighborhood of the drain region.

3. A semiconductor device according to claim 2, wherein the second conductivity type drift region is formed by implanting at least two kind second conductivity type impurities which have different diffusions coefficients and at least one kind first conductivity type impurity which has a diffusion coefficient substantially equal to or larger than the diffusion coefficient of at least one kind second conductivity type impurity such that it is formed by diffusing the second conductivity type impurities into a deep region by using a difference in the diffusion coefficients and is formed shallowly in a neighborhood of the source region by canceling the second conductivity type impurities by the first conductivity type impurity.

4. A semiconductor device according to claim 3, wherein the second conductivity type drift region is formed by implanting an arsenic ion and a phosphorus ion as the second conductivity type impurities into an overall surface of a region serving as the drift region and selectively implanting a boron ion as the first conductivity type impurity only into a region in a neighborhood of the source region.

8. A semiconductor device comprising a first MOS transistor having a source region, a channel region, a drain region, a gate electrode formed on the channel region, and a drift region formed between the channel region and the drain region, and a second MOS transistor having a source region, a channel region, a drain region, and a gate electrode formed on the channel region,

wherein the drift region of the first MOS transistor is formed shallowly at least below the gate electrode but formed deeply in a neighborhood of the drain region and

a source/drain region of the second MOS transistor consists of a low concentration source-drain region, a high concentration source-drain region, and a middle concentration source/drain region whose concentration is higher than that of the low concentration source/drain region but lower than that of the high concentration source/drain region.

9. A semiconductor device comprising a first MOS transistor and a second MOS transistor formed on a first conductivity type semiconductor substrate;

wherein the first MOS transistor includes,

a first conductivity type well region formed in the semiconductor substrate,

a first gate electrode formed on the first conductivity type well region via a first gate insulating film,

a first conductivity type body region formed to be adjacent to the first gate electrode,

a second conductivity type source region and a channel region formed in the first conductivity type body region,

a second conductivity type drain region formed at a position remote from the first conductivity type body region, and

a second conductivity type drift, region formed shallowly from the channel region to the drain region, at least below the gate electrode, and formed deeply in a neighborhood of the drain region, and

wherein the second MOS transistor includes,

a second conductivity type well region formed in the semiconductor substrate,

a second gate electrode formed on the second conductivity type well region via a second gate insulating film, and

a source/drain region consisting of a low concentration source/drain region formed to be adjacent to the second gate electrode, a high concentration source/drain region, and a middle concentration source/drain region whose concentration is higher than that of the low concentration source/drain region but lower than that of the high concentration source/drain region.

10. A semiconductor device according to claim 9, wherein the first MOS transistor consists of an N-channel LDMOS transistor, and the second MOS transistor consists of a P-channel high breakdown voltage MOS transistor.

17. A semiconductor device according to claim 1, wherein the semiconductor device is arranged in plural via a element isolation film, and

a channel stopper layer is formed under the element isolation film.

19. A semiconductor device according to claim 2, wherein the second conductive type drift region is formed to be adjacent to the first conductive type body region.